from transistors **102**, **106** and **104** and resistors **108** and **110**. In the embodiment of FIG. **1**, the trigger elements **114** and **116** each comprise a series of diodes **110** (1-N) and **112** (1-N). However, the trigger elements **114** and **116** could be any appropriate element that provides a trigger current when the desired voltage is reached. The desired voltage is the trigger voltage used to turn on the SCR. This is driven by the amount of isolation used (i.e., 1, 2, 3, 4 or 5V of ground to ground isolation). In operation, once the trigger elements **114** and **116** allow enough current to flow in the base/emitter junction of one or both of the bipolar transistors **102** or/and **104** to fully turn them on, the transistors **102** and/or **104** inject causing transistor **106** to turn on completing a self generation circuit. Further, in some embodiments, multiple layout versions are designed to optimize the trigger current, holding voltage and dynamic on resistance.

[0020] An example of an illustration of a structure of one embodiment of tunable voltage isolation ground clamp **235** is illustrated in FIGS. **2**A and **2**B. In particular, FIG. **2**A illustrates a partial cross-sectional view of a dual-direction SCR **200** of FIG. **1** without the trigger elements and FIG. **2**B includes trigger elements **240** (1-N). As illustrated in FIG. **2**A, a dual-direction SCR **200** includes two Pwells **218** and **220** separated by an Nwell/Niso **224**. The Nwell/Niso **224** is formed in a P substrate **226**. As illustrated, the structure is isolated from the substrate **226** by the N-type isolation region **224**. Each Pwell **218** and **220** has a P+ well tie **202** and **208** respectively and an N+ cathode region **204** and **206** respectively.

[0021] The dual-direction SCR **200** of FIG. **2**A includes a first and a second SCR. The first SCR is formed by N+ region **204**, Pwell **218**, Nwell **224**, and Pwell **220**. This SCR includes NPN transistor **210** and the PNP transistor **230**. The second SCR is formed by N+ region **206**, Pwell **220**, Nwell **224**, and Pwell **218**. This SCR includes NPN transistor **212** and the PNP transistor **230**. The Pwells **218** and **220** form resistances indicated by resistors **214** and **216** respectively, that are used to develop a voltage drop across the base (Pwell)/emitter(N+) of the NPN transistors.

[0022] Once sufficient current flows in the base/emitter junction of the transistors **210** and/or **212** to turn them on, the clamp **235** will trigger from a blocking state into a low conductive state (an "on" state). The holding voltage, dynamic resistance, and trigger current are defined by the spacing between the various layers that form the dual-direction SCR **200**. In particular, the holding voltage is the minimum voltage required to maintain the dual-direction SCR **200** in its on state. It is defined by a gain and collector resistance of the bipolar transistors that form the dual-direction SCR **200**. The spacing **221** between the two Pwells **218** and **220** is where the Nwell **223** is formed. This width **221** is the base width of the PNP transistor **230** and is also the collector resistance of the two NPN transistors **210** and **212**. The dynamic resistance is the differential resistance of the dual-direction SCR **200** while it is in the on state and the trigger current is the minimum current required to trigger the dual-direction SCR **200** into its on state. The range of these spacing are used to optimize the device for Ground to Ground protection.

[0023] In FIG. **2**B only one set of trigger elements **240** (1-N) are illustrated. As illustrated, the trigger elements **240** (1-N) are connected to Pwell **220** via P+ contact **232** to build up the base/emitter voltage of the NPN transistor once the selected voltage is reached. The other set of trigger elements (not shown) would be coupled similarly to Pwell **218**. As illustrated in FIG. **2**B, each trigger element **240** includes a P+ region **244** and a N+ region **246** formed in a Nwell **242**. The Nwell **242** is formed in a Psub **248** that isolates the diode from the dual-direction SCR **200**. As discussed above, the clamp **235** is tunable by varying the number of the trigger elements **140** (1-N) used.

[0024] FIG. **3** illustrates a schematic diagram of a of a tunable voltage isolation ground clamp **300** of another embodiment of the present invention. In this embodiment, trigger junction zener diodes **306** and **308** are used. Zener diodes **306** and **308** breakdown at a specific voltage. When the breakdown voltage is reached, they supply the base current that is required to turn the SCR on. The tunable voltage isolation ground clamp **300** also includes NPN transistors **302** and **304**, a PNP transistor **310** and resistors **312** and **314** as illustrated.

[0025] FIG. **4** illustrates a tunable voltage isolation ground clamp **400** formed in a substrate **428** of one embodiment of the schematic diagram illustrated in FIG. **3**. In the embodiment of FIG. **4**, overlapping N+/P+ regions **414**, **416** and **418** and **420** at the Nwell/Pwell **426**, **422** and **424** edges are used to initiate triggering. These are the zener diodes of FIG. **3**. As also illustrated in FIG. **4**, the ground clamp **400** also includes Pwells **422** and **424** formed in Nwell **426**. Each Pwell **422** and **424** has a P+ well tie **402** and **408** respectively and an N+ cathode region **404** and **406** respectively. The NPN transistors **302** and **308** of FIG. **3** are formed by N+ cathode region **404**, Pwell **422** and Nwell **426** and N+ cathode region **406**, Pwell **424**, and Nwell **426** respectively. The PNP transistor **310** of FIG. **3** consists of the two Pwells **422** and **424** separated by Nwell **426** of FIG. **4**. The Nwell **426** is formed in P substrate **428**. The Pwells **422** and **424** form resistances indicated by resistors **312** and **314** respectively, that are used to develop a voltage drop across the Base (Pwell)/emitter(N+) of the NPN transistors **310**.

[0026] A voltage difference develops between the two grounds (GND**1** positive with respect to GND**2**). The voltage of the P+(**402**), PWELL (**422**) increase forward biasing of the Zener diode (**414**) thereby biasing the NWELL (**426**). The voltage increases until the Zener diode (**412**) breaks down injecting current into the PWELL (**424**). Once this occurs, current flows through the PWELL (**424**) wherein a voltage is developed in the PWELL (**424**) resistance. Once this voltage reaches ~0.7 v, the NPN formed by the NWELL/PWELL (**424**)/N+(**406**) turns on. This in turn, turns on the SCR switching it from the blocking state to the conductive (on state). In a similar manner, a positive voltage on GND**2** would initiate turn-on of the NPN transistor formed by the NWELL/PWELL (**422**)/N+(**404**) transistor. Once sufficient current flows, the clamp will trigger going into a low conductive state.

[0027] Referring to FIG. **5**, a Transmission Line Pulse (TLP) graph **500** that shows the result of a tunable clamp of one embodiment is illustrated. The units of measure of the TLP graph **500** include voltage in volts along the bottom axis, current in amps along the side axis and current in amps along the top axis. In creating the TLP graph, a rectangle current pulse is forced into the device and the resulting voltage on the device is measured. The voltage and current is represented by the circles that make up the V/I characteristic curve **504** for the ESD element. The voltage and current are indicated by the voltage scale along the bottom axis and the current scale along the side axis of the graph. After each current pulse, a leakage current measurement is taken to monitor if the device has failed. The current leakage measurement tells how much